

Patent claims

1. Method for programming a memory module (104) by stimulating individual inputs (CS, OE, WR, ADDR, DATA) of the memory module (104) via at least one memory cell (103) of a Boundary Scan (BSCAN) register (102), characterized by
5 the exclusive control of the control signal input (WR) of the memory module (104) responsible for activating or deactivating a write operation, where the switchover of a WRITE ENABLE signals (301d) from "LOW" to "HIGH" potential or from "HIGH"
10 to "LOW" potential is undertaken as a function of an instruction sequence (301a), which ensures that at inputs of an update flip-flop (108) of the memory cell (103) which is responsible for generating the WRITE ENABLE signal a "LOW" or a "HIGH" level is generated.
- 15 2. Method according to Claim 1, characterized in that the "LOW" or "HIGH" levels at the inputs of the update flip-flop (108) of the memory cell concerned (103) of the BSCAN register (102) can be generated in any given timing sequence.
- 20 3. Method in accordance with one of the Claims 1 and 2, characterized in that
The timing sequence of the "LOW" or. "HIGH" levels at the setting signal or reset signal input of the update flip-flop (108) of the memory signal involved (103) of the BSCAN
25 register (102) is controlled by the instruction sequence (301a).

4. Method in accordance with one of the Claims 1 to 3,
characterized in that
the signals for the update-flip-flop (108) of the memory cell
concerned(103) are generated by a control unit (106) as a
5 function of the instruction sequence (301a).

5. Method for programming a memory module (104) through
stimulation of individual inputs (CS, OE, WR, ADDR, DATA) of
the memory module (104) via at least one memory cell (103) of
a BSCAN register (102) to generate a WRITE_ENABLE signal
10 (301d) for the purposes of activating or deactivating a write
operation,
characterized by
the automatic switchover of the WRITE_ENABLE signal (301d)
from "LOW" to "HIGH" potential or from "HIGH" to "LOW"
15 potential by a control unit (106) at a suitable point in time,
by an update flip-flop (108) setting or resetting the memory
cell (103) responsible for the generation of the WRITE_ENABLE
signal.

6. Method according to Claim 5,
20 characterized in that
the automatic generation of a setting signal (SET_WR) for
activating the write operation can be activated by the control
unit (106) using a programming command (EXFLASH).

7. Method according to Claim 6,
25 characterized in that
the automatic generation of the setting signal (SET_WR) can be
prevent if specific instructions (EXTEST or SHORTEX) are
present.

8. Method according to Claim 5,
characterized by
a further instruction (WR_ON), with which the control unit
(106) can be notified that a setting signal (SET_WR) for
5 activating the write operation is to be automatically
generated.
9. Method according to one of the Claims 5 and 8,
characterized by
a further instruction (WR_OFF), with which the control unit
10 (106) can be notified that a reset signal (CLEAR_WR) for
deactivating the write operation is to be automatically
generated.
10. Method according to Claim 5,
characterized in that
15 the suitable point in time for automatic switchover of the
WRITE_ENABLE signal (301d) is programmed by means of suitable
instructions.
11. Control unit for control of individual memory cells (103)
of a BSCAN register (102) via a programming interface, which,
20 when programming a memory module (104) is used for stimulating
individual inputs (CS, OE, WR, ADDR, DATA) of the memory
module (104) via at least one memory cell (103) for initiating
or ending a write operation,
characterized in that
25 it is designed for execution of a method in accordance with
one of the Claims 1 to 10.
12. Memory cell of a BSCAN register (102), which is used when
programming a memory module (104) for stimulation of

individual inputs (CS, OE, WR, ADDR, DATA) of the memory module (104) for the purposes of initiating or ending a write operation, characterized in that

5 it is designed for execution of a method in accordance with one of the Claims 1 to 10.

13. BSCAN register, consisting of a number of memory cells (103) for control of a programmable memory module (104), which is used for stimulation of individual inputs (CS, OE, WR, ADDR, DATA) of the memory module (104) for the purposes of
10 initiating or ending a write operation, characterized in that it is designed for execution of a method in accordance with one of the Claims 1 to 10.